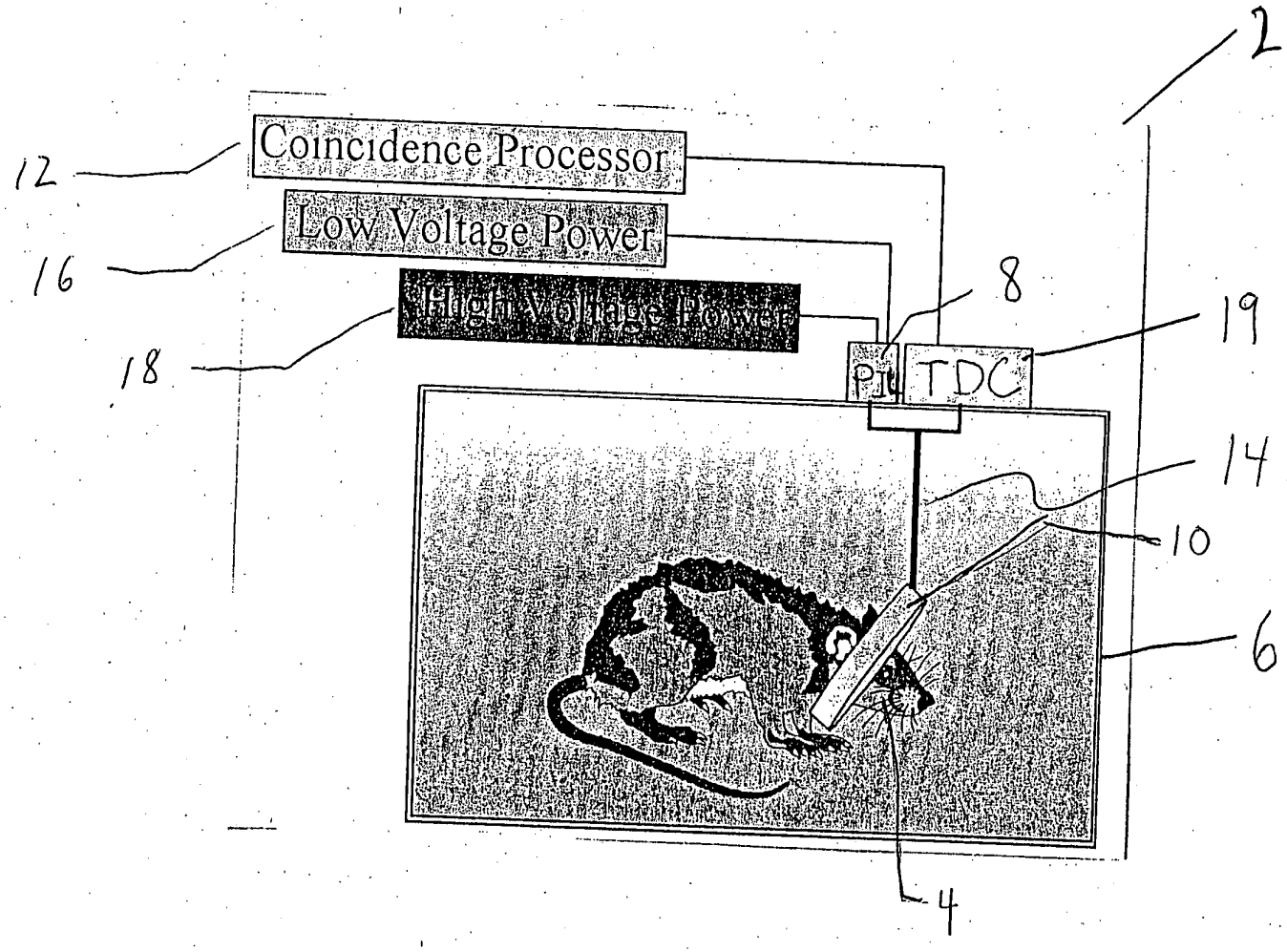

2
12
Coincidence Processor
16
Low Voltage Power
18
High Voltage Power
8
19
PU
TDC
14
10
6
4

Figure 1.

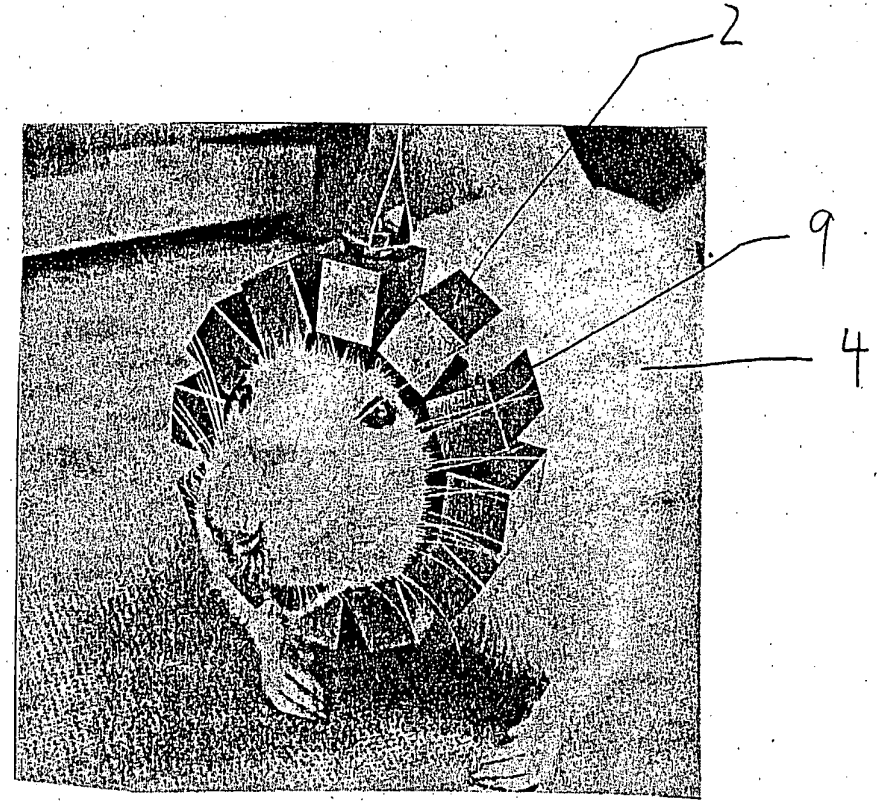


Figure 2

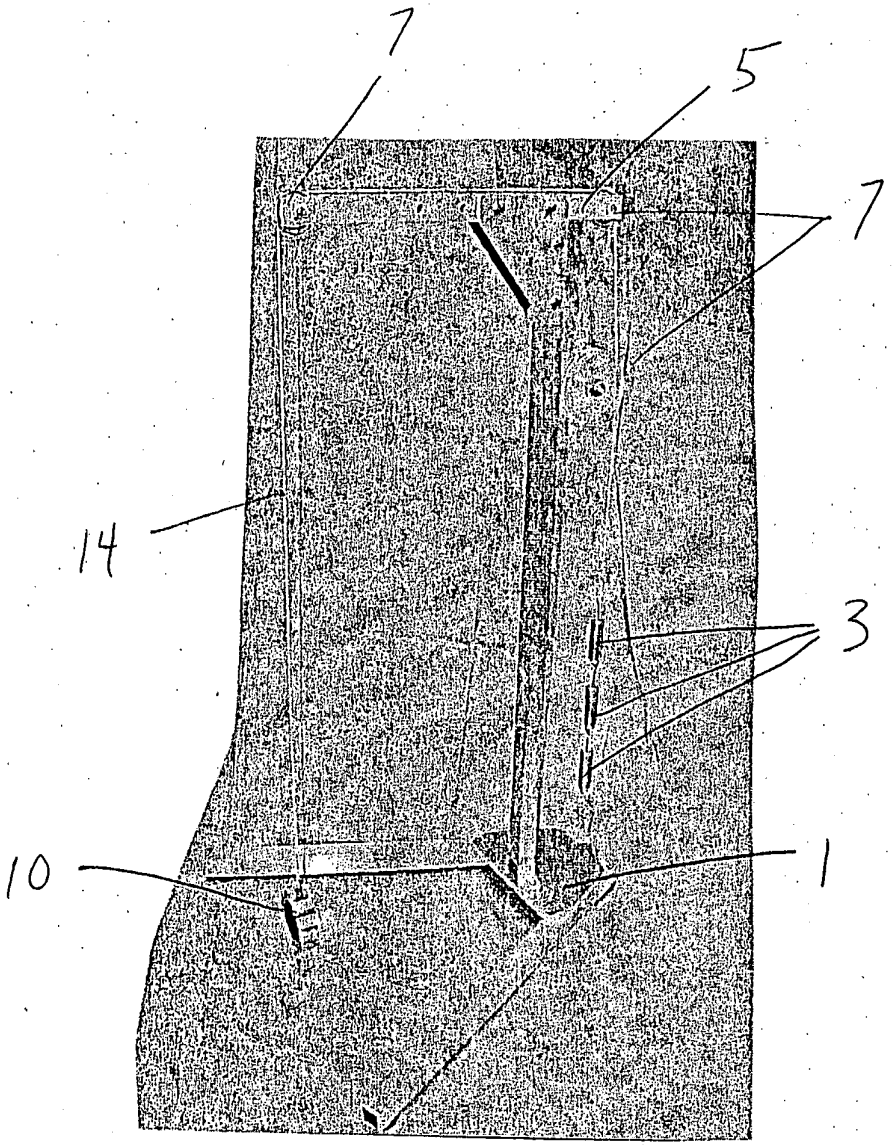


Figure 3a

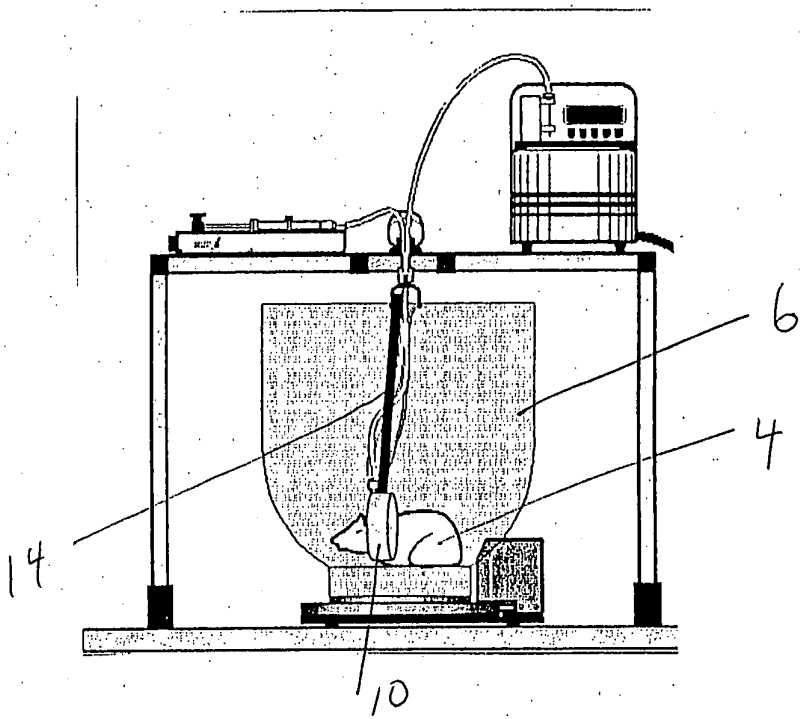


Figure 3b

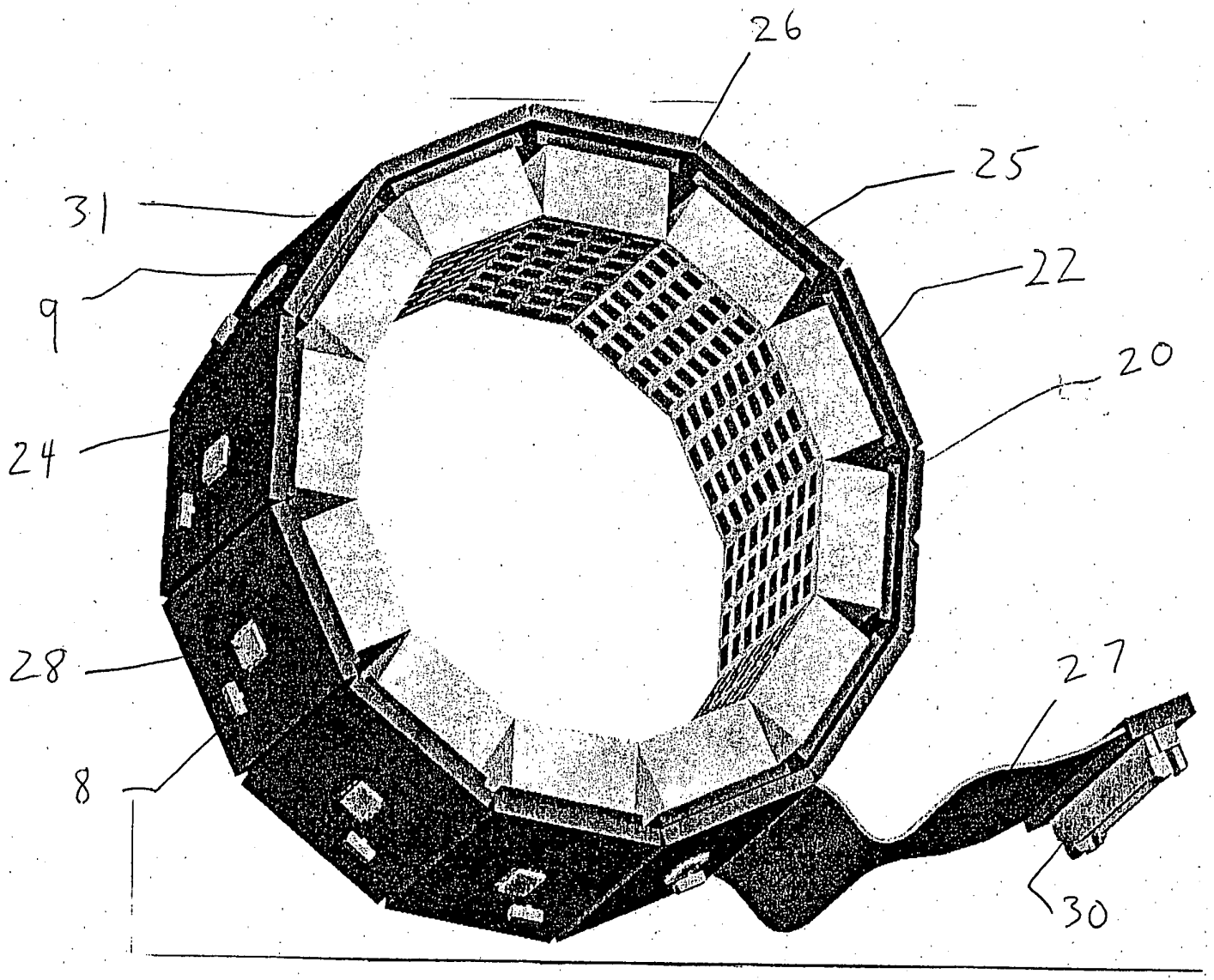


Figure 4

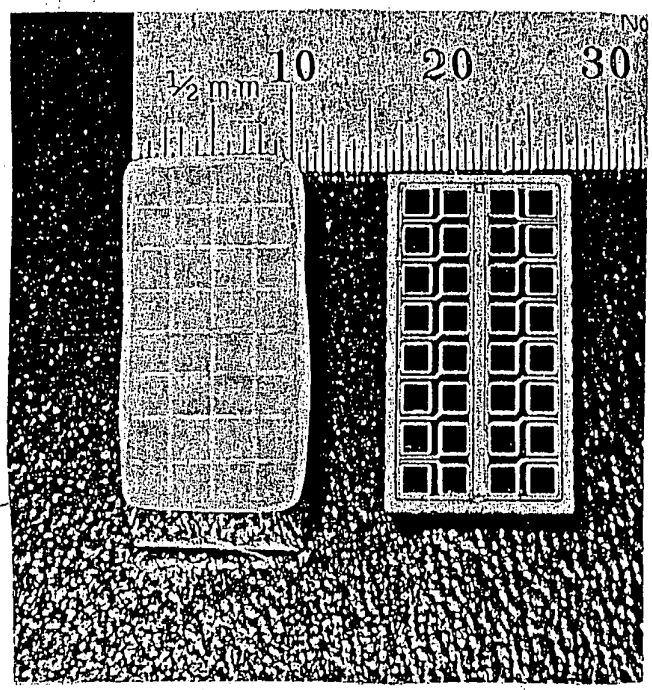


Figure 5

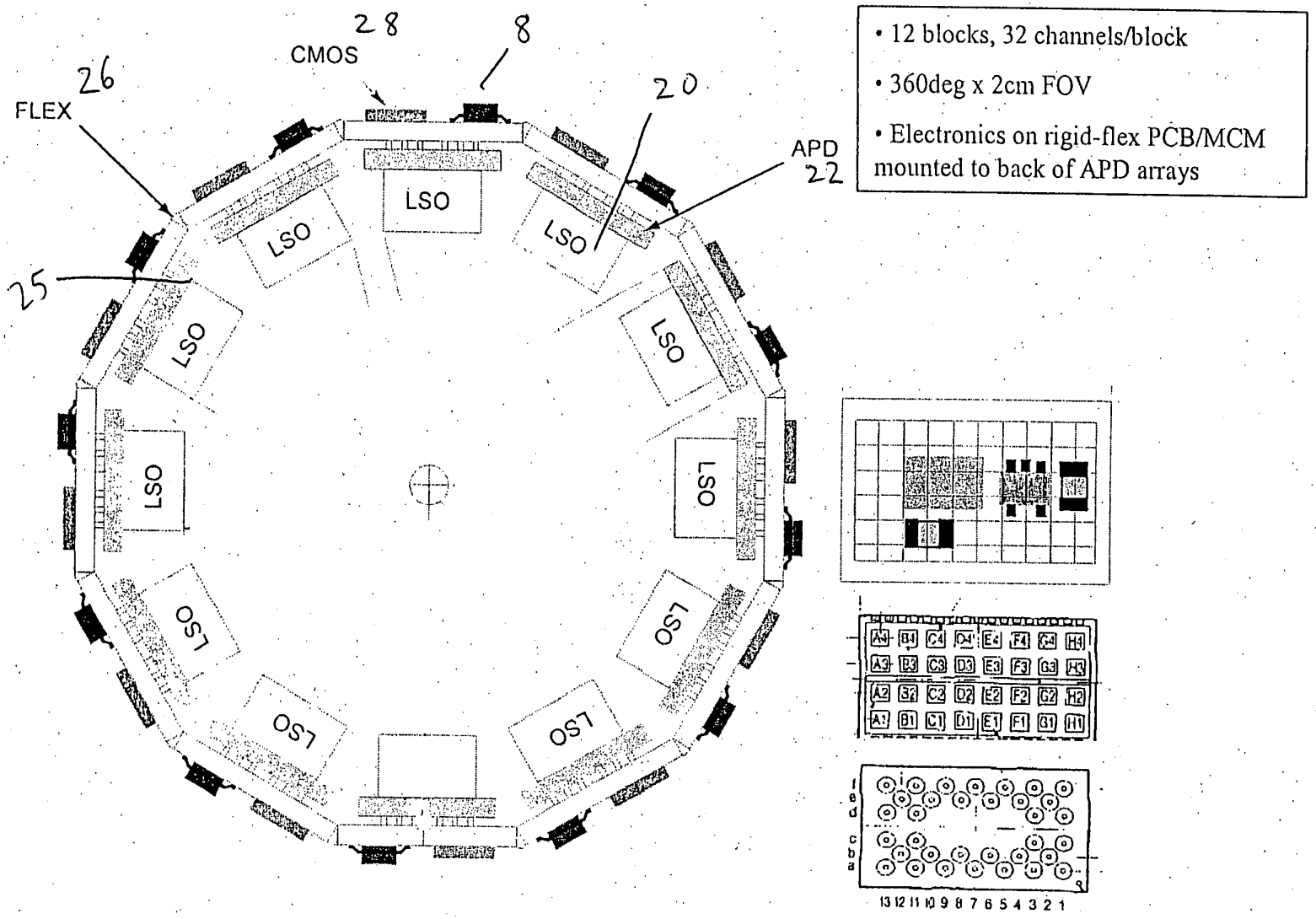

28
CMOS
8
26
FLEX
20
APD
22
25
LSO
• 12 blocks, 32 channels/block
• 360deg x 2cm FOV
• Electronics on rigid-flex PCB/MCM mounted to back of APD arrays

Figure 6

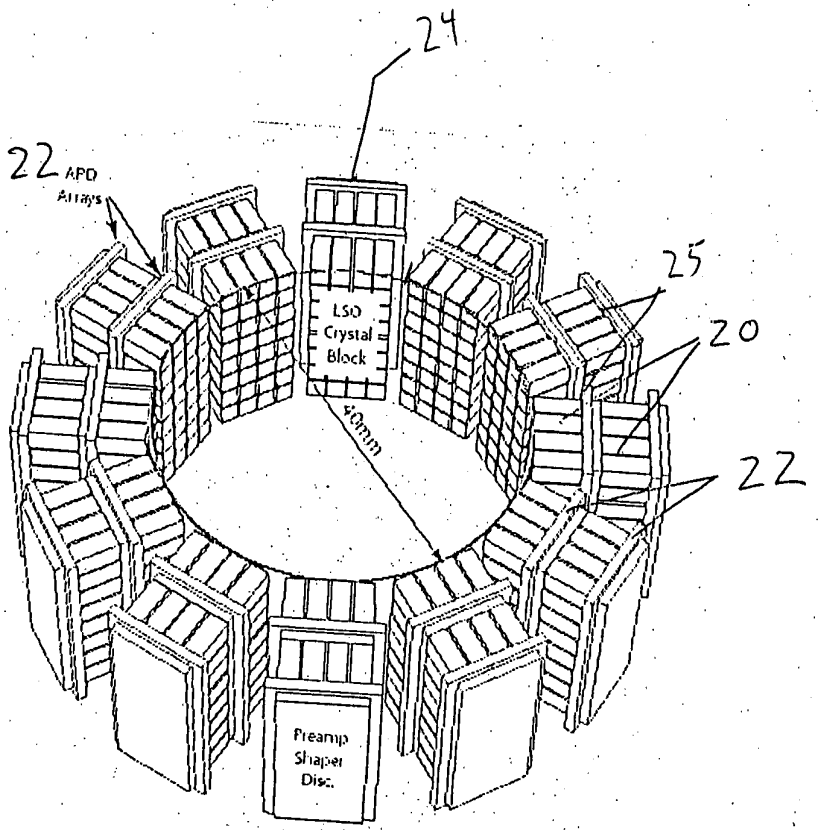

24
22 APD Arrays
25
20
22
LSO Crystal Block
40mm
Preamp Shaper Disc.

Figure 7.

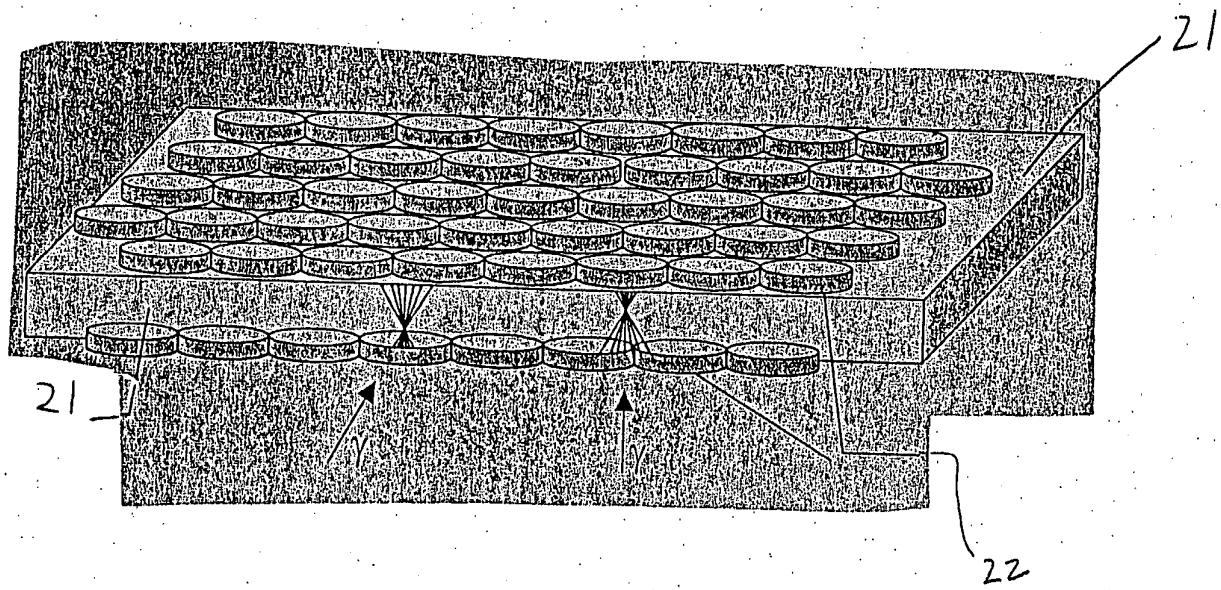


Figure 8.

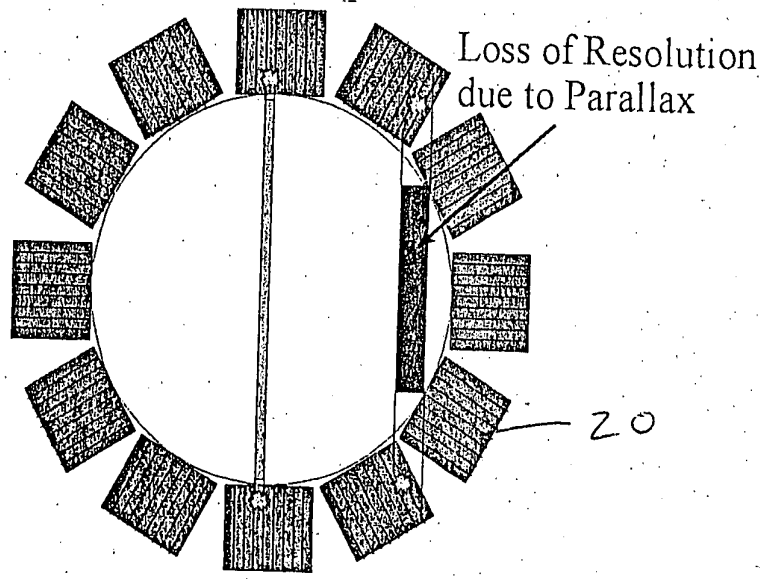


FIGURE 9a

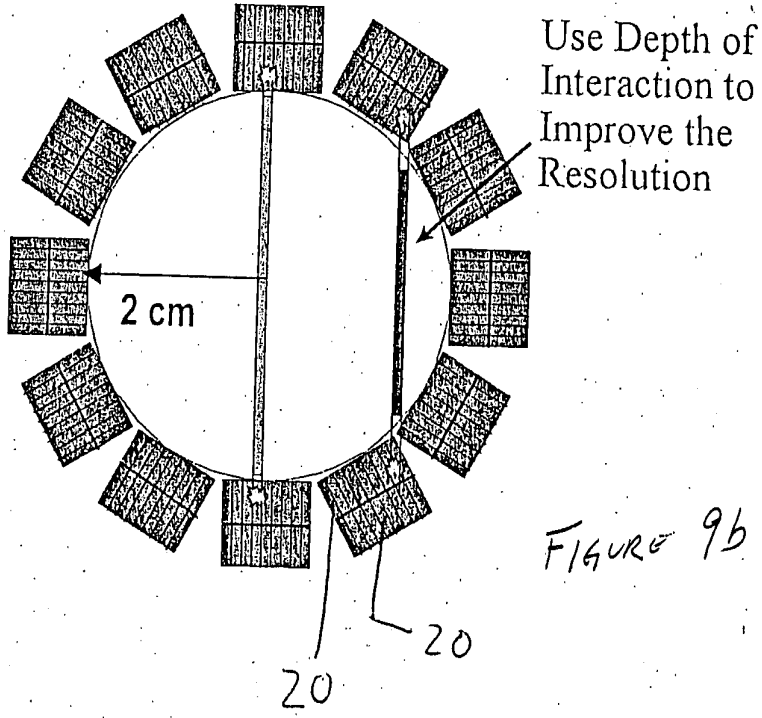


FIGURE 9b

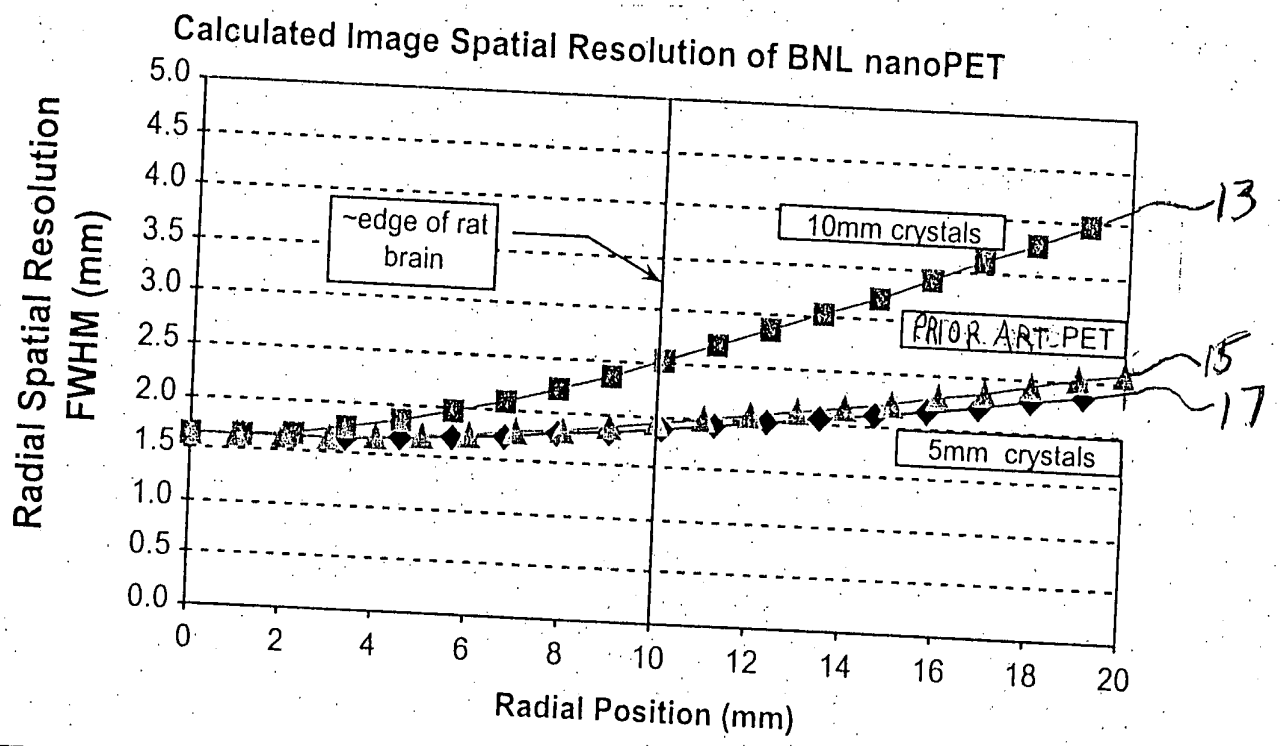

Calculated Image Spatial Resolution of BNL nanoPET
Radial Spatial Resolution FWHM (mm)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
2
4
6
8
10
12
14
16
18
20
Radial Position (mm)
~edge of rat brain
10mm crystals
PRIOR ART PET
5mm crystals
13
15
17

Figure 10

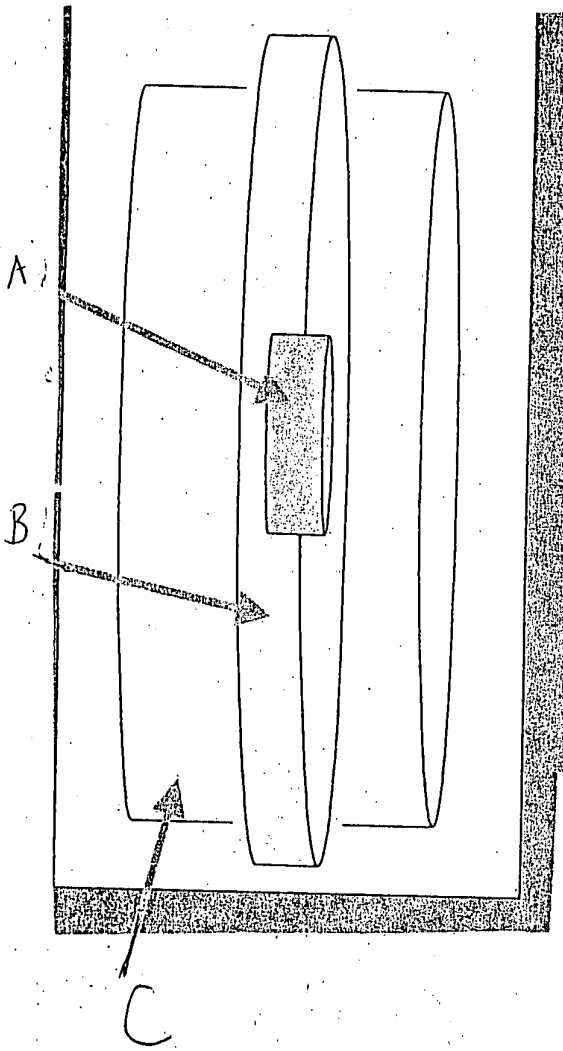


Figure 11a

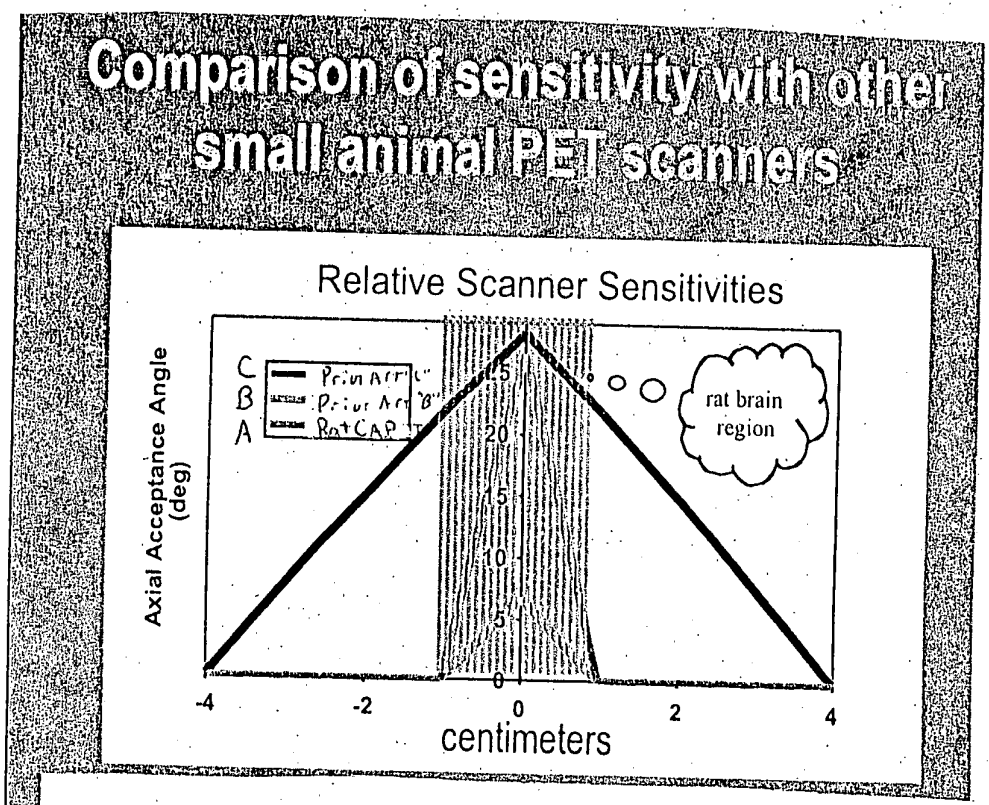


Figure 11b

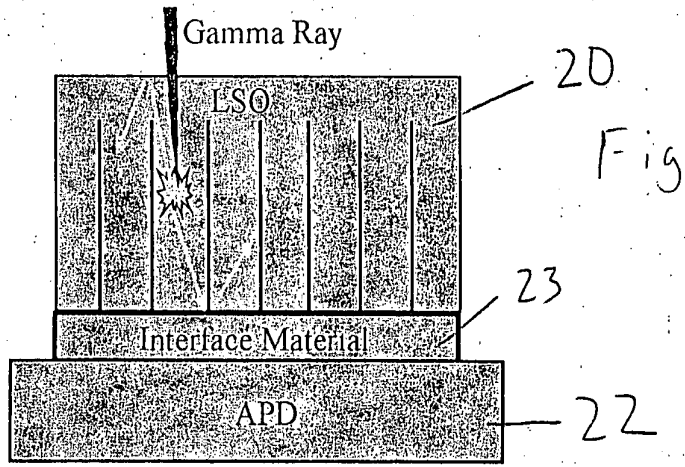


Figure 12a

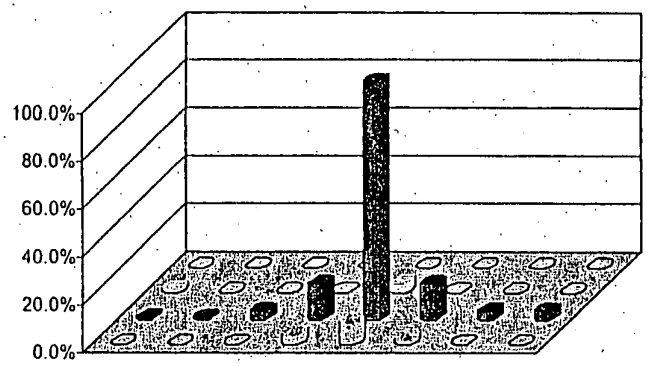


Figure 12b

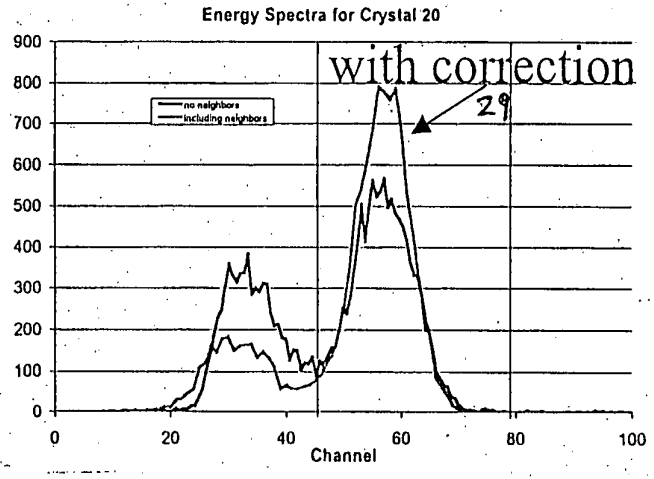


Figure 12c

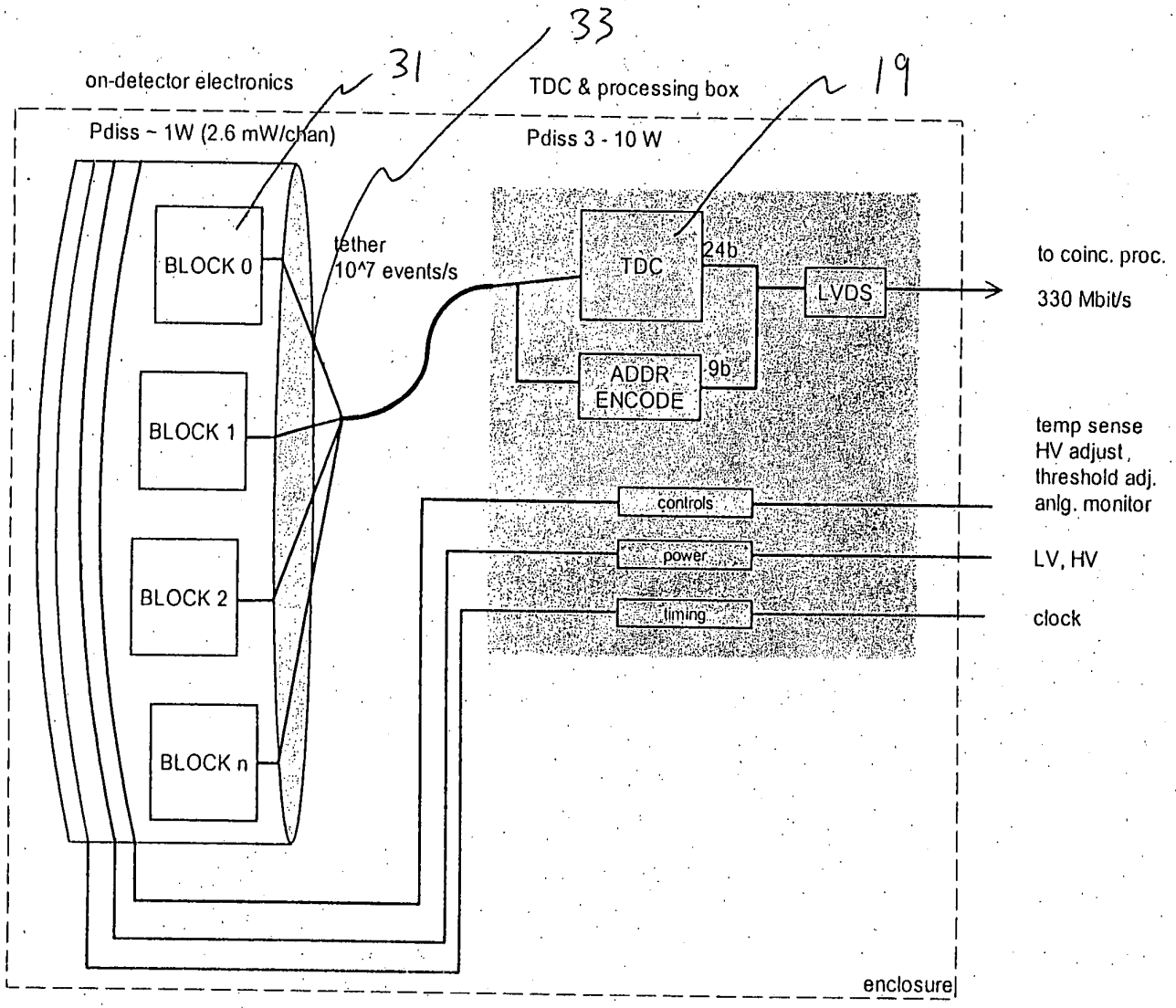

33
31
19
on-detector electronics
Pdiss ~ 1W (2.6 mW/chan)
TDC & processing box
Pdiss 3 - 10 W
BLOCK 0
BLOCK 1
BLOCK 2
BLOCK n
tether
10^7 events/s
TDC
24b
LVDS
ADDR ENCODE
9b
controls
power
timing
to coinc. proc.
330 Mbit/s
temp sense
HV adjust,
threshold adj.
anlg. monitor
LV, HV
clock
enclosure

Figure 13

individual serial links

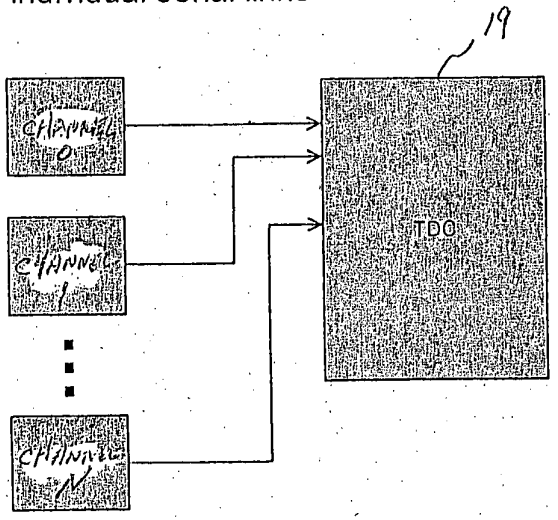


FIGURE 14a
PRIOR ART

common serial bus with busy

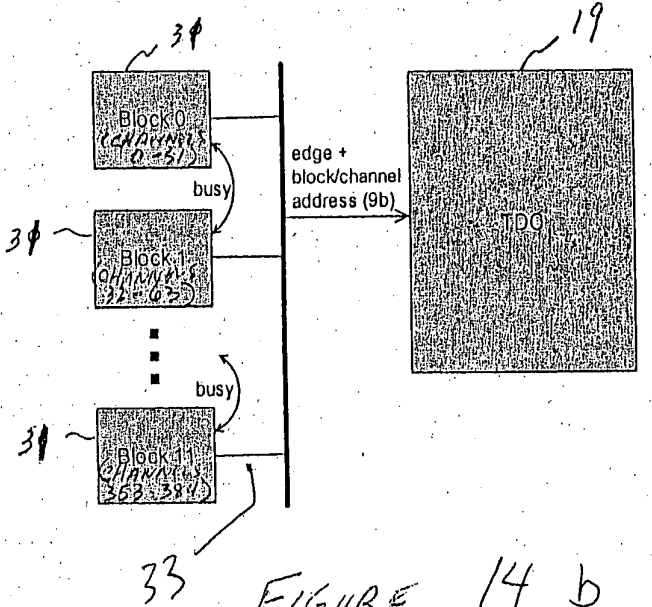
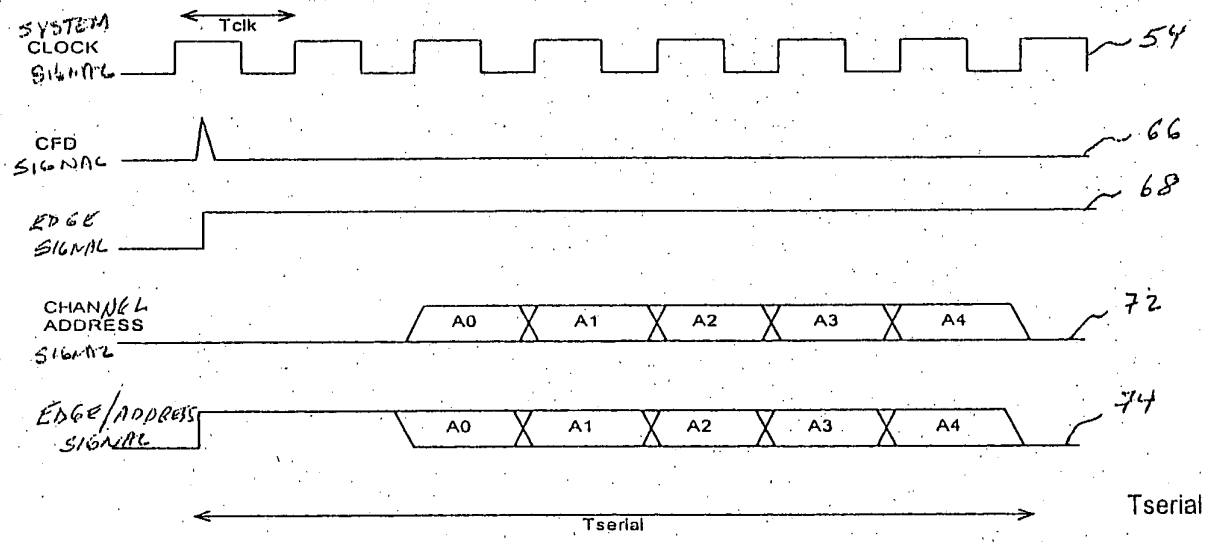


FIGURE 14b

Serial link timing



Tserial = (nbits + 2) * Tclk

FIGURE 15

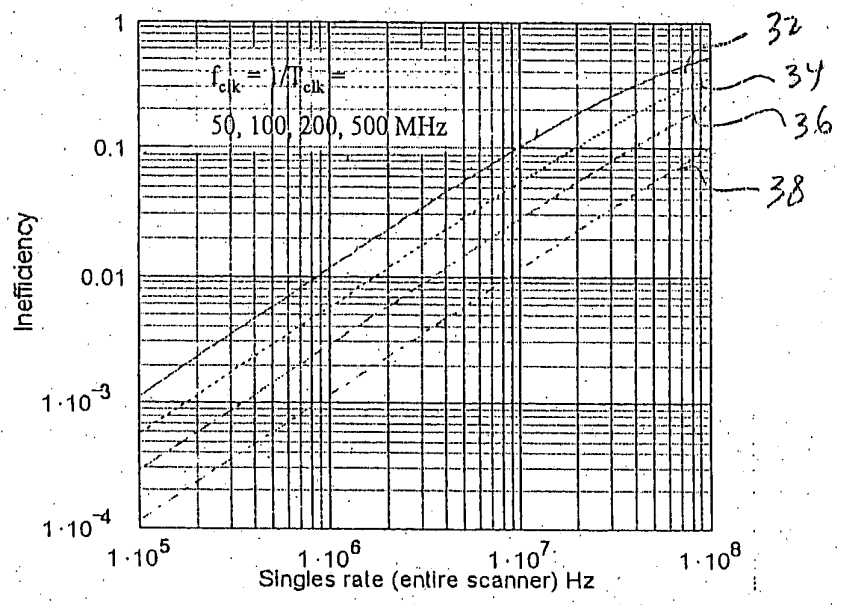

1
0.1
0.01
1·10^-3
1·10^-4
Inefficiency
f_clk = 1/T_clk =
50, 100, 200, 500 MHz
32
34
36
38
1·10^5
1·10^6
1·10^7
1·10^8
Singles rate (entire scanner) Hz

FIGURE 16

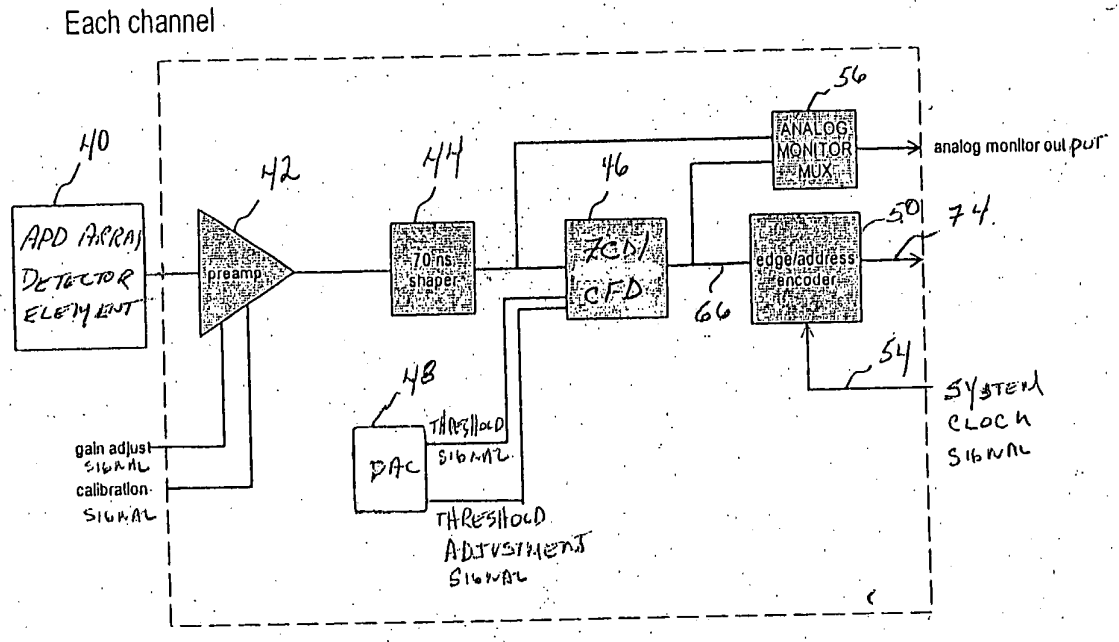

Each channel
40
APD ARRAY DETECTOR ELEMENT
42
preamp
44
70ns shaper
46
ZCD/ CFD
56
ANALOG MONITOR MUX
analog monitor output
50
74
edge/address encoder
66
54
SYSTEM CLOCK SIGNAL
48
DAC
THRESHOLD SIGNAL
THRESHOLD ADJUSTMENT SIGNAL
gain adjust SIGNAL
calibration SIGNAL

FIGURE 17

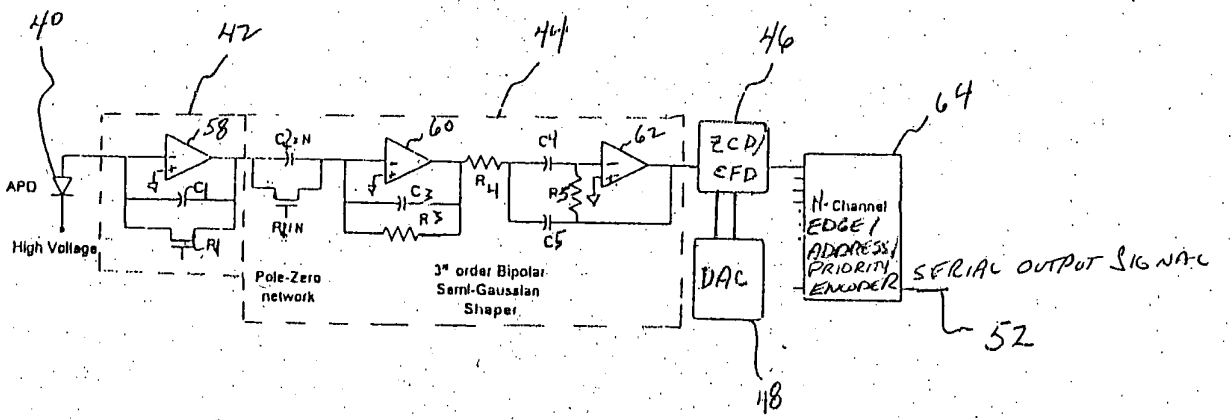

40
42
44
46
64
58
60
62
APD
High Voltage
C1
R1
C2 N
RLIN
C3
R3
R4
C4
R5
C5
ZCD/
CFD
DAC
N-Channel
EDGE/
ADDRESS/
PRIORITY
ENCODER
SERIAL OUTPUT SIGNAL
52
48
Pole-Zero
network
3rd order Bipolar
Semi-Gaussian
Shaper

FIGURE 18

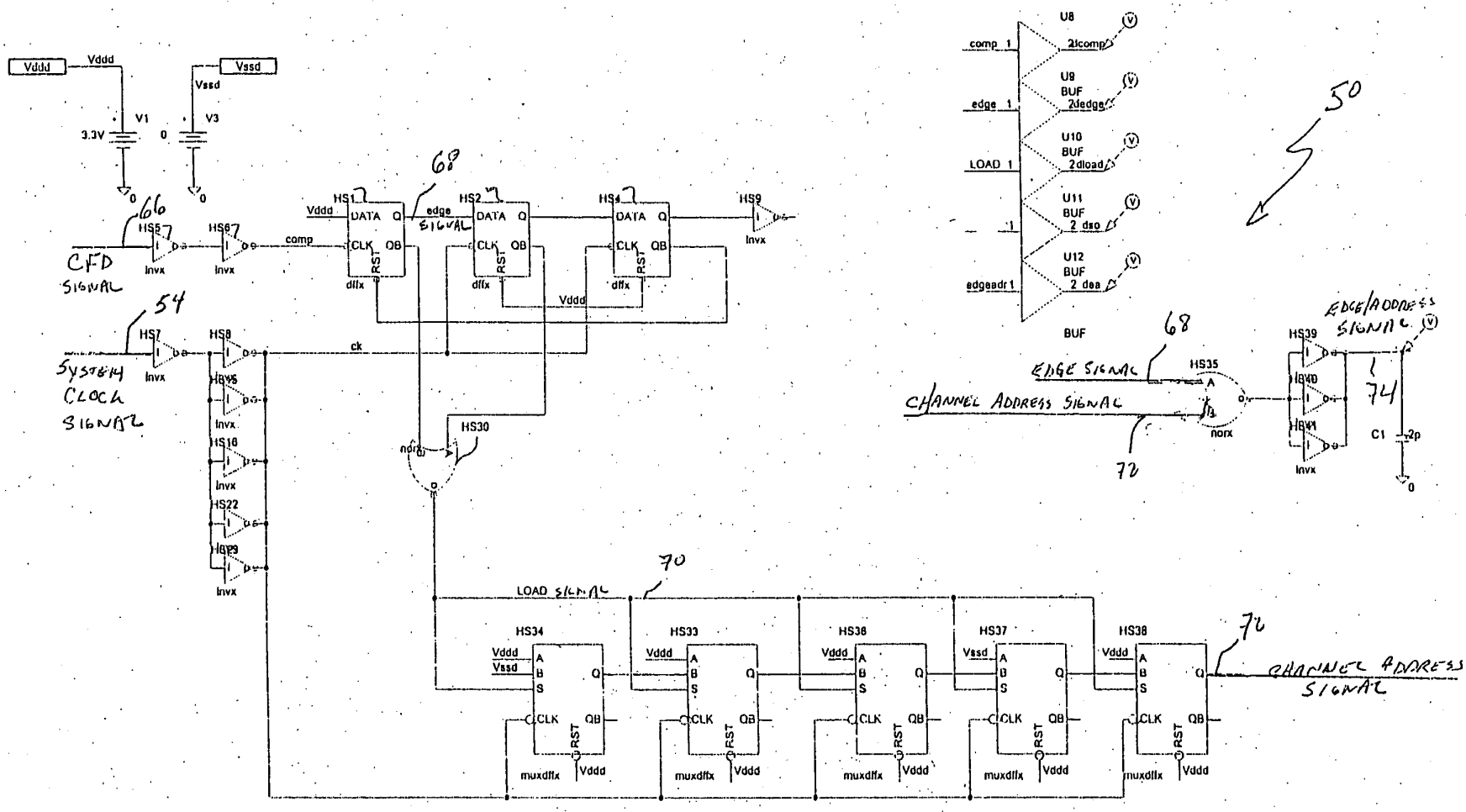
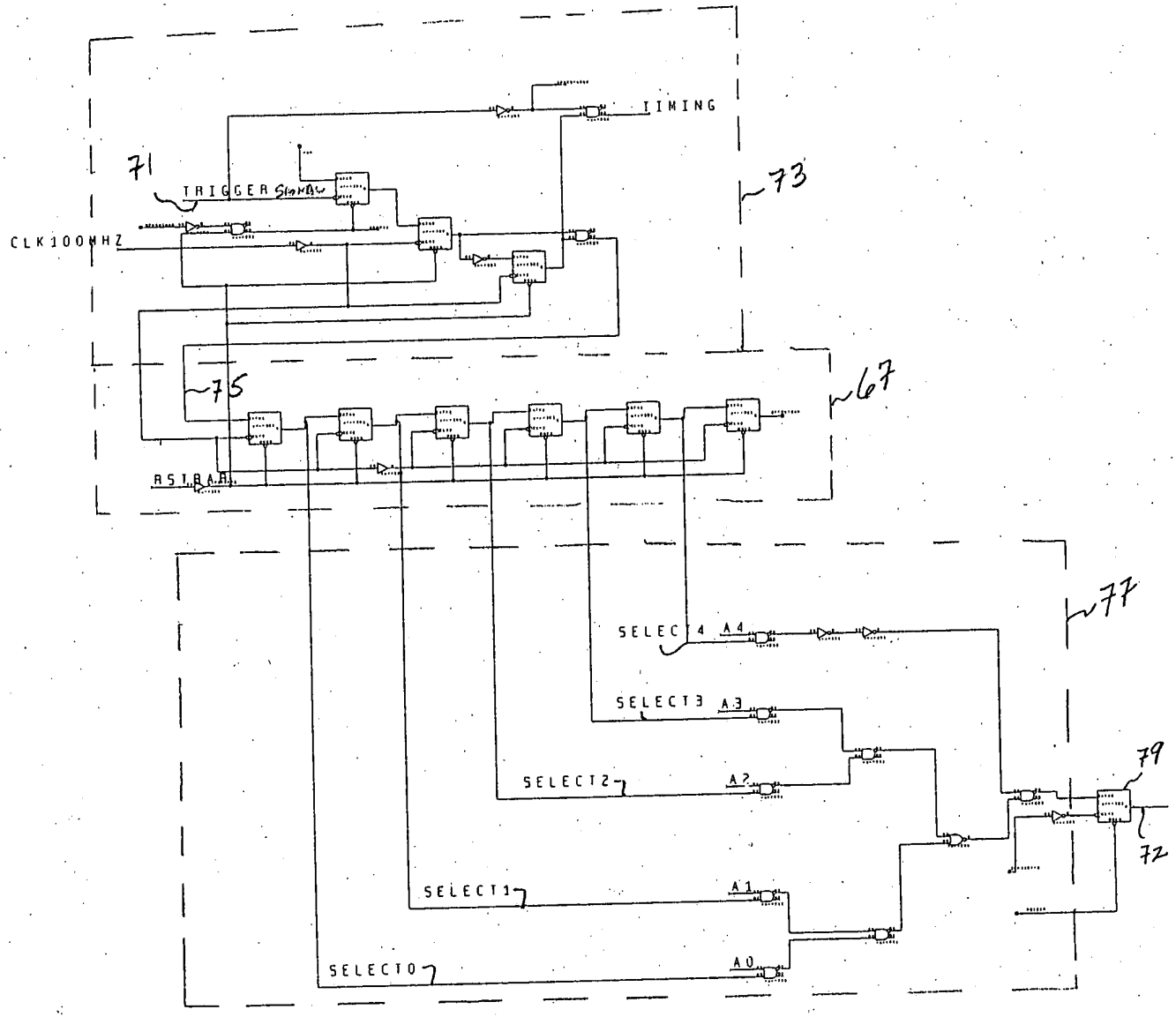

Vddd
Vssd
V1
V3
3.3V
0
CFD SIGNAL
66
HS5
HS6
Invx
comp
HS1
HS2
HS4
HS9
DATA
CLK
QB
RST
dffx
edge SIGNAL
68
54
HS7
HS8
SYSTEM CLOCK SIGNAL
ck
HS15
HS16
HS22
HS29
HS30
nor
LOAD SIGNAL
70
HS34
HS33
HS36
HS37
HS38
muxdffx
72
CHANNEL ADDRESS SIGNAL
U8
2icomp
U9
BUF
2iedge
U10
2iload
U11
2 dso
U12
2 dea
comp_1
edge_1
LOAD_1
edgeadr1
50
EDGE SIGNAL
HS35
norx
HS39
EDGE/ADDRESS SIGNAL
74
C1
2p

FIGURE 19



TRIGGER=Asynchronous Trigger

A[4:0]-5 Bit Crystal ID from the 32 to 5 Priority Encoder

SERADD=serialized 5 bit Crystal ID at 100MHz

FIGURE 19a

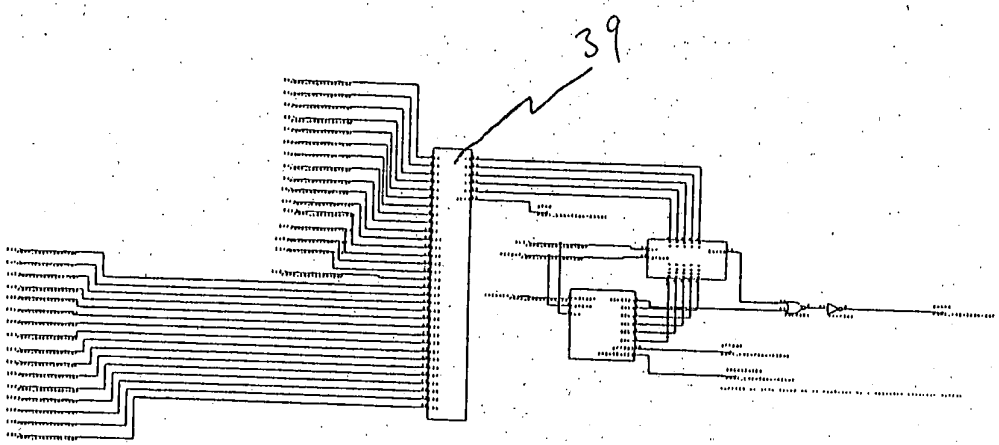


FIGURE 20

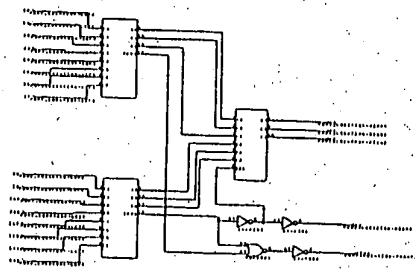


FIGURE 21

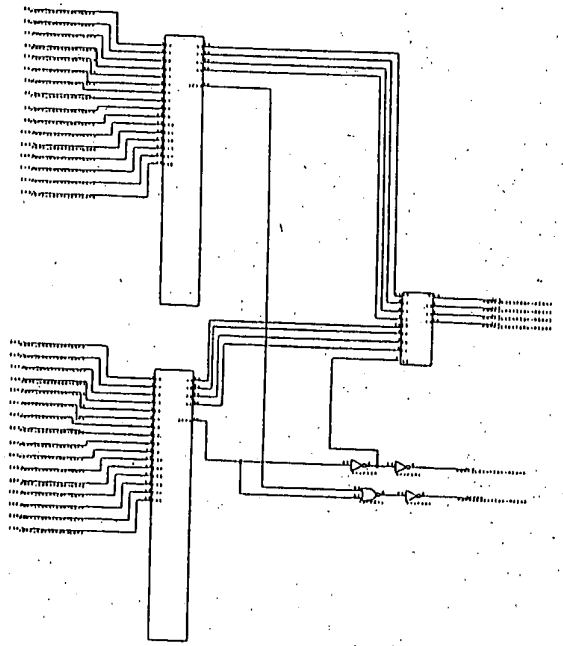


FIGURE 22

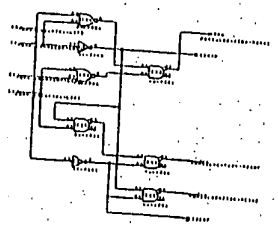


FIGURE 23

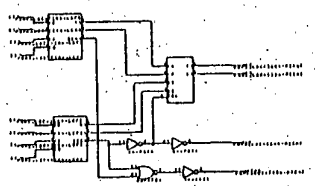


FIGURE 24

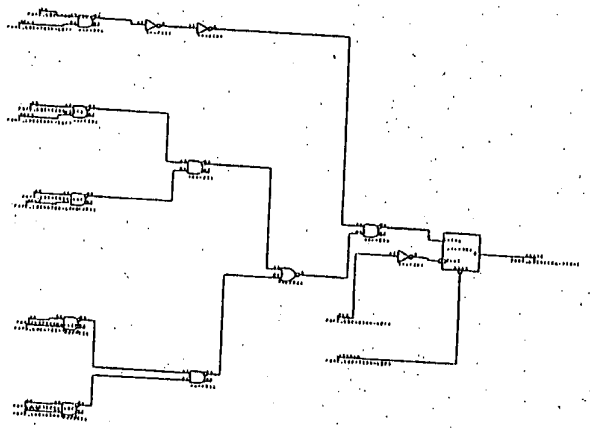


FIGURE 2-25

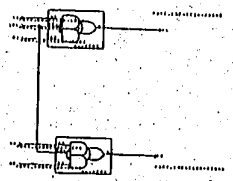


FIGURE 26

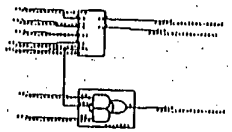


FIGURE 207

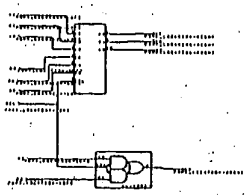


FIGURE 2.8

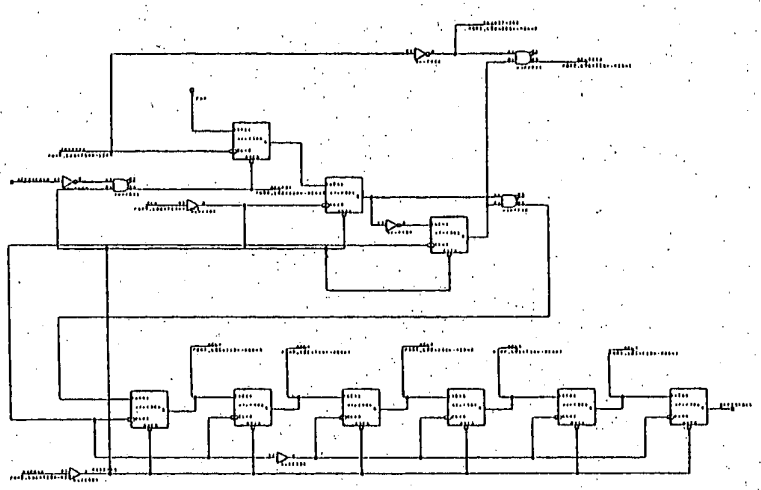


FIGURE 2.9

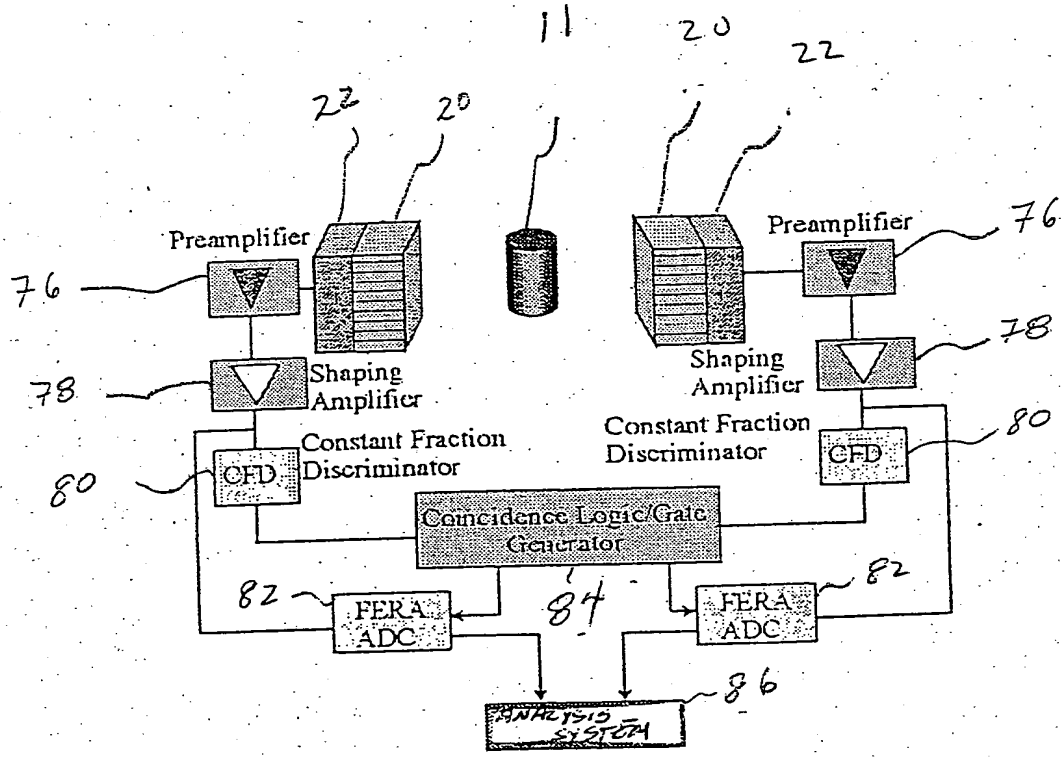

11
20
22
22
20
Preamplifier
76
76
Preamplifier
78
Shaping Amplifier
78
Shaping Amplifier
80
CFD
Constant Fraction Discriminator
Constant Fraction Discriminator
CFD
80
Coincidence Logic/Gate Generator
82
FERA ADC
84
FERA ADC
82
ANALYSIS SYSTEM
86

FIGURE 30

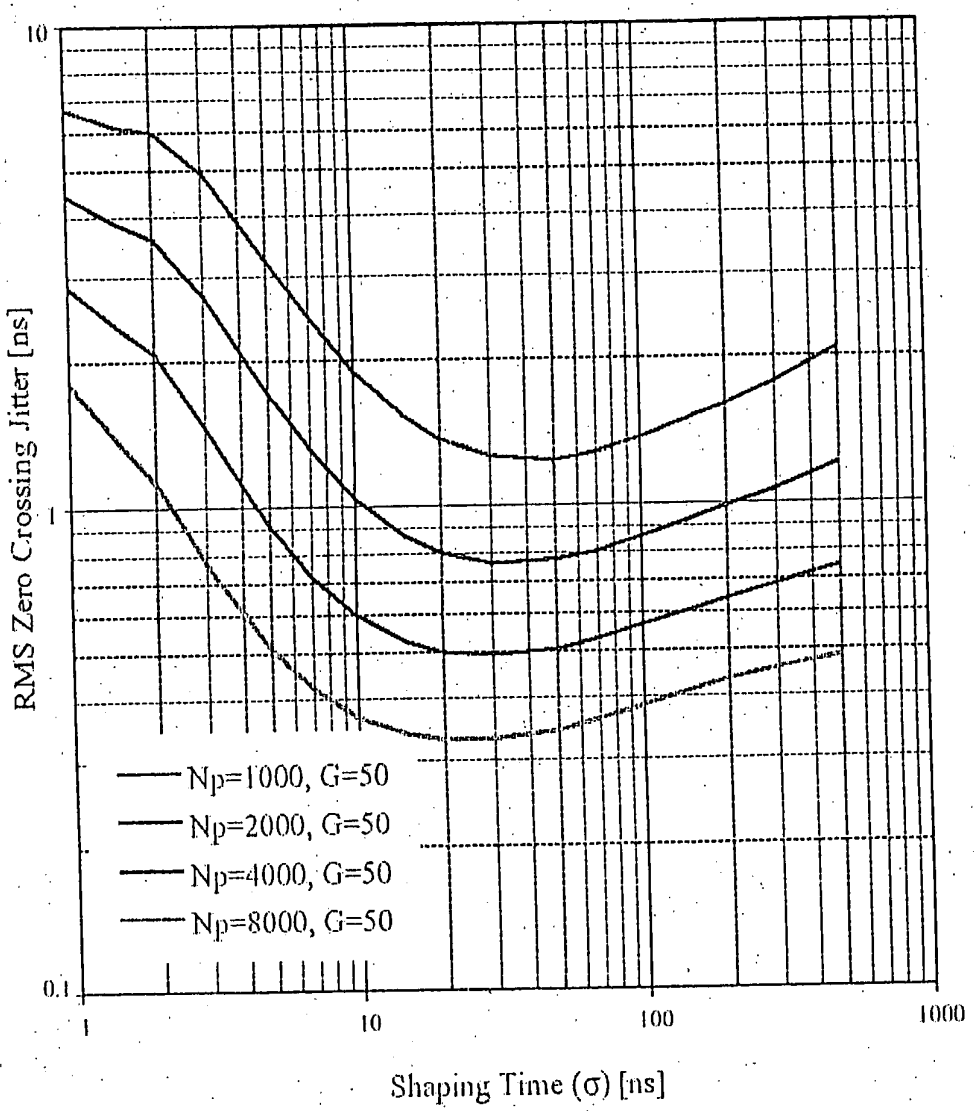

10
1
0.1
RMS Zero Crossing Jitter [ns]
Np=1000, G=50
Np=2000, G=50
Np=4000, G=50
Np=8000, G=50
1
10
100
1000
Shaping Time (σ) [ns]

FIGURE 31

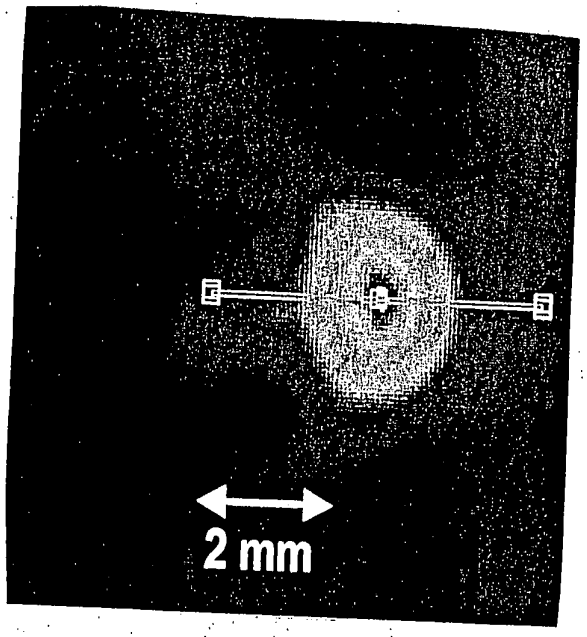


Figure 32 a

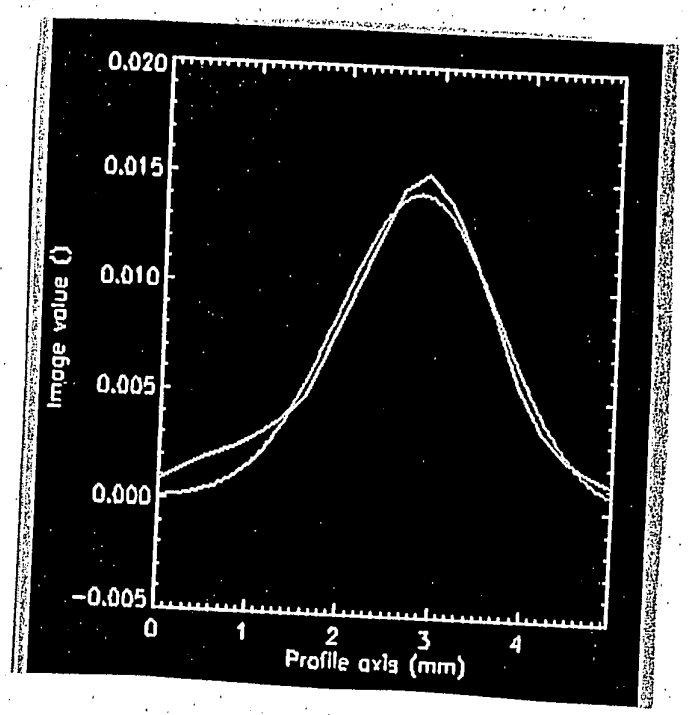


Figure 32 b

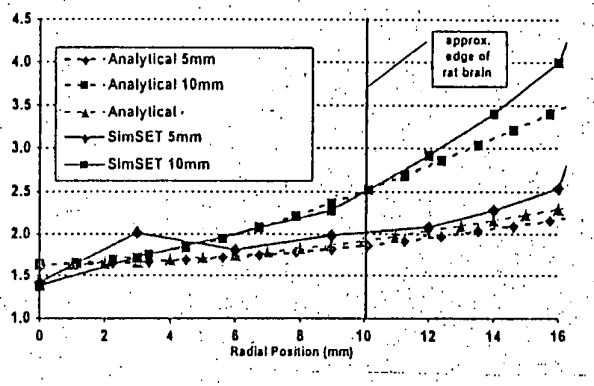

4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0
2
4
6
8
10
12
14
16
Radial Position (mm)
Analytical 5mm
Analytical 10mm
Analytical
SimSET 5mm
SimSET 10mm
approx. edge of rat brain

Figure 33.

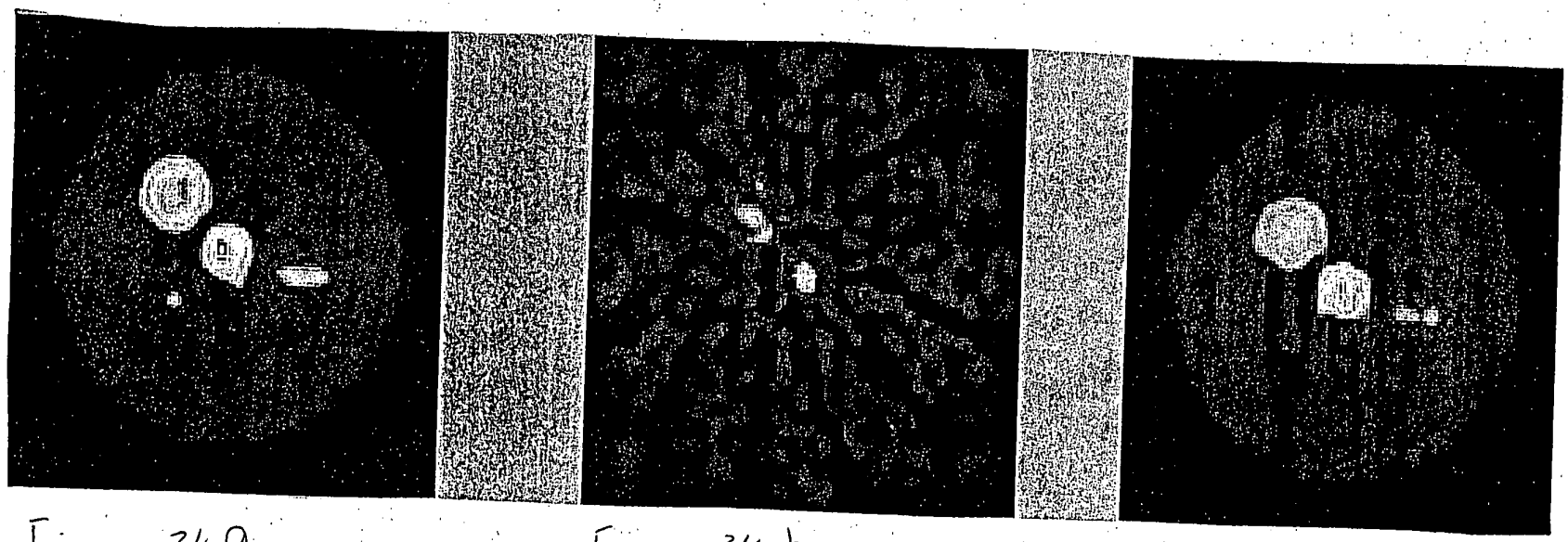


Figure 34a

Figure 34b

Figure 34c